UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/636,000	08/09/2000	Stephen P. Pope	20669-000300US	5413

20350 7590 03/01/2004

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/01/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/636,000	POPE, STEPHEN P.	
	Examiner	Art Unit	
	Kevin M Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-10* is/are allowed.

6)☒ Claim(s) *1-5,7,11 and 12* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the amendment filed 1/2/2004, is a final office action.

Response to Arguments

2. The previous objections to the specifications and claims are withdrawn.

3. The previous rejection of claim 1 under 35 USC 102(b) is withdrawn due to the amendment. A new rejection under 35 USC 103(a) is stated below for claim 1, necessitated by the amendment.

Applicant's arguments filed 1/2/2004 have been fully considered but they are not persuasive. Regarding claims 1-5 and 7, Applicant states the combination of Cooper and Beat do not disclose means for computing supporting branch metric parameter calculations wherein branch metric parameters are computed recursively for a sequence of states, wherein said recursive computation requires only a single addition operation per branch metric parameter per state. Cooper discloses a trellis of states and paths are associated with the possible transmitted symbol sequence in figure 1. The branch metrics are determined by the formulas shown in column 5, line 53 to column 6, line 33. As stated in the previous office action, Cooper doesn't disclose computing the branch metric parameter calculations with a Grey code. Beat discloses this in column 2, lines 22-33. The Grey code has the property that only one bit of the binary sequence is changed in going from one state to the next. The combination teaches calculating a

branch metric parameter by changing only one bit (a single addition). For these reasons and the reasons stated previously, the rejections of the claims are maintained.

Regarding claims 11 and 12, Applicant states the combination of Jekal and Beat do not disclose providing a trellis, providing a present state and incrementing the present state to the next state by changing only one bit. Jekal discloses providing a trellis and providing a present state and a next state as stated in the previous office action and shown in Jekal, column 1, lines 33-58. Jekal does not explicitly disclose only changing one bit in the present state to form a next state. Beat discloses a method of changing one binary sequence to another binary sequence by changing only one bit of that sequence (column 2, lines 22-33). By changing states of the binary sequence by changing only one bit on any one transition, components of the circuit are eliminated and the effective speed of the circuit is increased (column 2, lines 28-33). For these reasons and the reasons state below, the rejections of claims 11 and 12 are maintained.

Claims 8-10 are allowed. Claim 6 is objected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper (US 5,502,735) in view of Beat (US 5,687,352).

Regarding claims 1 and 2, Cooper discloses a maximum likelihood sequence detector (title) for estimating a sequence of transmitted symbols received over a communication channel (column 1, lines 6-10). A trellis of states and paths are associated with the possible transmitted symbol sequences (figure 1). The detector comprises a plurality of data sources relating to state transition probabilities and observed values of received data symbols (abstract). Means for calculating and storing the likelihood metric and the survivor bit for each state of the trellis is disclosed in column 3, lines 54-61. This data is read out of storage to estimate the most likely sequence of transmitted data. This reading step is commonly known in the art as "trace-back" (column 3, lines 61-64). The largest partial path metric is selected at the final stage of the trellis (column 10, lines 63-65). This is the final state. Cooper does not disclose computing the branch metric parameter calculations with a Gray code. Beat discloses a method of changing one binary sequence to another binary sequence by changing only one bit of that sequence using a Gray code (column 2, lines 22-33). By changing states of the binary sequence by changing only one bit on any one transition, components of the circuit are eliminated and the effective speed of the circuit is increased (column 2, lines 28-33). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the method of changing transitions of Beat into the detector of Cooper.

Regarding claim 3, Cooper discloses the branch metric parameters are pre-computed and stored in memory prior to the forward trace through the trellis (column 6, lines 5-9).

Regarding claim 7, Copper discloses inputting partial path metrics to MUX 46 in figure 7 to generate soft decision data 44 (column 15, line 59 to column 16, line 3).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper (US 5,502,735) in view of Beat (US 5,687,352) further in view of Murakami (US 5,440,588).

Regarding claim 4, the combination of Cooper and Beat disclose the detector stated above in paragraph 4. The combination does not disclose the branch metric parameters are calculated in real time. Murakami discloses conventional maximum likelihood sequence estimation uses a large amount of real time calculations to calculate the branch metrics and the final sequence (column 5, lines 14-56). Murakami further discloses a method of eliminating some of these real time calculations in the disclosure. It would have been obvious for one of ordinary skill in the art at the time of the invention to use the teachings of Murakami in the combination of Cooper and Beat. The use of real time calculations in calculating the branch metrics is a conventional method of calculating branch metrics and is beneficial since it eliminates the memory used to store the pre-computed branch metric values. No memory is needed for these calculations in real time.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper (US 5,502,735) in view of Beat (US 5,687,352) further in view of Hladik et al (US 5,721,746).

Regarding claim 5, the combination of Cooper and Beat discloses the maximum likelihood sequence detector as stated above in paragraph 4. The combination does not disclose calculating "valid" initial states representing prior knowledge about the transmitted sequence for use in the decoder. Hladik discloses using prior information to calculate the probabilities of the initial starting states (column 7, lines 56-63). The information about the states is stored in registers (column 3, lines 8-17). Any state with at least a probability of being the starting state must be used to insure the correct sequence is output and therefore is a "valid" starting state. It would have been obvious for one of ordinary skill in the art at the time of the invention to utilize the teachings of Hladik in the decoder of Cooper and Beat to remove the starting states of the trellis that have no probability of being the initial starting state. To use these states would be a waste of resources.

7. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jekal (US 6,035,428) in view of Beat (US 5,687,352).

Regarding claim 11, Jekal discloses a method for computing a maximum likelihood sequence estimate comprising providing a trellis comprising nodes corresponding to a plurality of states at a plurality of stages (column 1, lines 34-65). The present state and next state comprises a series of bits (column 1, lines 41-48). Jekal

does not disclose incrementing the present state to a next state by changing only one bit. Beat discloses a method of changing one binary sequence to another binary sequence by changing only one bit of that sequence (column 2, lines 22-33). By changing states of the binary sequence by changing only one bit on any one transition, components of the circuit are eliminated and the effective speed of the circuit is increased (column 2, lines 28-33). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the method of changing transitions of Beat into the method of Jekal.

Regarding claim 12, Beat discloses Gray code is used to increment the present state to a next state (column 2, lines 22-33).

Allowable Subject Matter

8. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 8-10 are allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications; please mark "EXPEDITED PROCEDURE" or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
2/26/2004

KHAI TRAN
PATENT EXAMINER